

**AUO**

**Display Specification for B133EW07 V1**

**13.3" Wide (1280x800) TFT-LCD**

**LED Backlight with High Color Gamut**

## Revision History

<u>DATE</u>	<u>REV #</u>	<u>Section #</u>	<u>CHANGE DESCRIPTION</u>

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DWG Number: **069-3542 Rev.01**

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## 1. General Description

This document establishes the requirements for the display device for the B133EW07 V1

<u>Category</u>	<u>Parameter</u>	<u>Specification</u>
<b>General</b>	Manufacturer	AUO
	Mfg. P/N	B133EW07 V1
	LCD TYPE	Normally-White, Transmissive TN TFT-LCD
	Diagonal	13.282" (33.74cm)
	Pixel Format	1280 (RGB stripe, H) x 800 (V)
	Pixel Pitch	0.2235(V) x 3x0.0745(H) mm
	Color Depth	18-bits (6R, 6G, 6B), 262144 colors
	Pooling requirement	Rigid Post Spacer with strong pooling resistance
	Packaging	Protective film on front polarizer. Displays packaged and air-tight sealed in anti-static bags.
	<b>Electrical</b>	Interface
Power Consumption		4.36 W @ Black (typical, the logic plus the backlight @94% duty cycle @23mA, 3.3V forward bias voltage)
<b>Optical</b>	Luminance	275 nits @ 94% duty cycle @23 mA (typical center)
	White LED Backlight	6 strings, 9 LED per string. Nichia NNSW208
	Hot Spots	No visible hot spot at any angle
	Viewing Direction	6:00 for worst dark inversion (pcb driver on the bottom)
	Contrast	500 typical
	Top Polarizer	Glossy Surface, 3H Hard Coating, LT4/ARC7 AR coating
	Diffuser Sheet	Tsujiden D153GS (top) & Tsujiden D120 (Bottom)
	BEF Sheet	2 X BEF2-G2 MR (Halogen free)
	Reflector	E6SR or equivalent (sulfur free)
	LGP	PMMA
<b>Mechanical</b>	Active Area	286.08 mm (H) x 178.80 mm (V)

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	Minimum Viewing Area	288.08 mm (H) x 180.80 mm (V)
	Module Outline Size	297.150 mm (H) x 192.150 mm (V)
	Connector	<b>IPEX 20474-030E-12</b>
	Mating Connector	<b>IPEX 20472-030T-10</b>
	Weight	300 grams typical
<b>Environmental</b>	Operating Temperature	0°C ~ +50°C
	Storage Temperature	-25°C ~ +65°C
<b>Pre-Aging</b>	Before shipment	Minimum 2 hours at 50°C, panel on

## 2. ORDER OF PRECEDENCE OF DOCUMENTATION AUTHORITY

In the case of any conflict in any specification related to these parts, this order of precedence of authority shall apply:

- 2.1. The Purchase Order
- 2.2. This Specification
- 2.3. Reference Documents

### 3. PHYSICAL DESCRIPTION

#### 3.1. Display Mode

Normally White, Transmissive, Twisted Nematic Liquid Crystal Displays

#### 3.2. Pixel Configuration

RGB Vertical Stripe

#### 3.3. Pixel Pitch

0.2235 mm x 0.2235 mm

#### 3.4. Resolution

1280 (RGB stripe, H) x 800 (V)

#### 3.5. Aperture Ratio

Minimum > 50%

#### 3.6. Optimum Viewing Cone

6 o'clock worst dark inversion direction (PCB on the bottom)

#### 3.7. Interface & Driving Scheme

3.3V single-channel LVDS (Flat Link) interface, requiring Hsync and Vsync signals, along with DE (Data Enable) mode, 2-dot inversion

#### 3.8. Front Surface Treatment

Low-reflection gloss surface, ~1% Reflectance,  $\geq 3H$  hardness (Sumitomo LT4, or Nitto Denko ARC7)

#### 3.9 Environmental Requirements:

Any homogeneous component must meet Halogen-Free Specification, 069-1857.



## 4. MECHANICAL REQUIREMENTS

### 4.1. Dimensions and Tolerances

The LCD module outline is described in the following table.

Dimension	Min	Typ	Max	Unit
Horizontal (H)	296.85	297.15	297.45	mm
Vertical (V)	191.85	192.15	192.45	mm
Depth (D)	3.08	3.38	3.68	mm

### 4.2. Weight

300 g (typical), 310 g (max)

### 4.3. Stack-up (tentative)

Mechanical Stack-up	Part #	Thickness /mm
Top Polarizer (glossy, LT4 or ARC7)	Sumika, SRW862APK-LT4	0.215
LCD Glass CF		0.5
LCD Glass TFT		0.5
Bottom Polarizer		0.215
Total Design Gap	-	0.135
Upper Diffuser	Tsujiden D131S	0.095
Upper BEF (Halogen Free)	BEF II-GII MR	0.155
Lower BEF (Halogen Free)	BEF II-GII MR	0.155
Lower Diffuser	Tsujiden D120	0.12
Light Guide	PMMA	0.72
White Reflector (Sulfur-free reflector for PMMA backlight)	E6SR	0.188
Rear Bezel	SUS 304	0.3
Tape		0.1
<b>Total Typical Thickness</b>	<b>w/o PCB</b>	<b>3.38</b>
Maximum Tolerance		0.3
<b>Total Maximum Thickness</b>	<b>(w/o PCB)</b>	<b>3.68</b>
PCB Thickness (8 Layer PCB)		0.8
Maximum Component - 1 side (include Solder)		1.15

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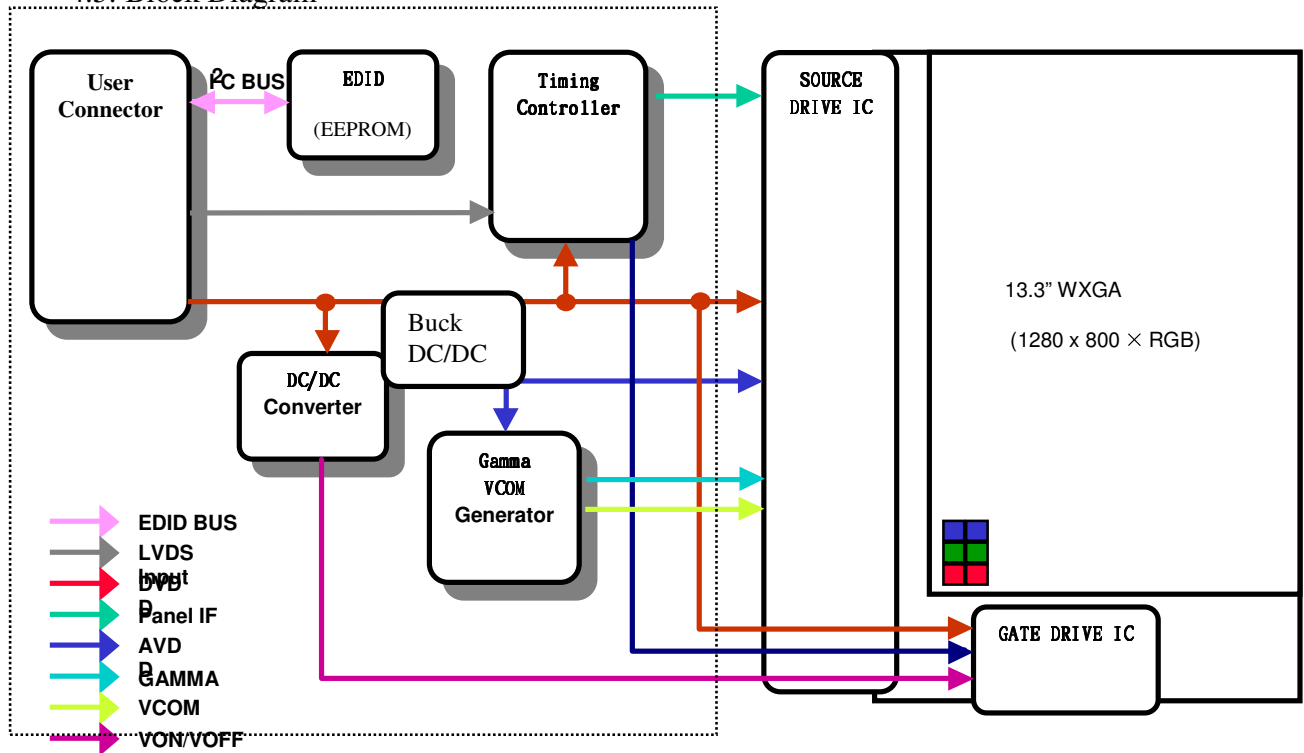
Maximum Component - 2 side (include Solder)		0.2
Total Maximum PCB Thickness		2.15

#### 4.4. Exposed Areas and Restrictions

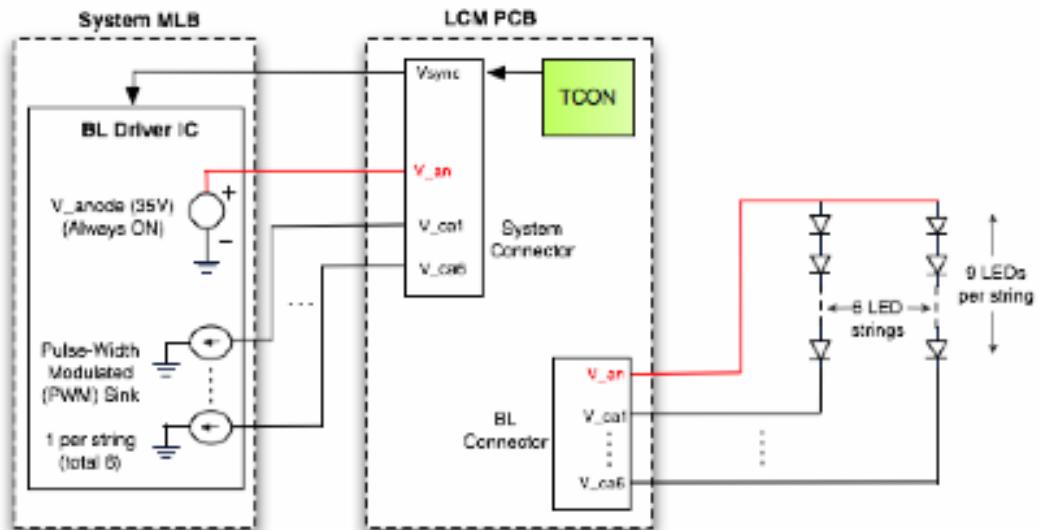
The display module shall not have exposed edges or components, which may cause injury or damage during handling, inspection, assembly, and service. Exposed areas of the display module (those not protected or shielded by construction) must be insulated and otherwise protected to eliminate the possibility of electrical shorting or destructive ESD discharges (per Section 7.2) during handling, inspection, assembly, and service.

# ELECTRICAL REQUIREMENTS

## 4.5. Block Diagram



## Backlight Driving Architecture



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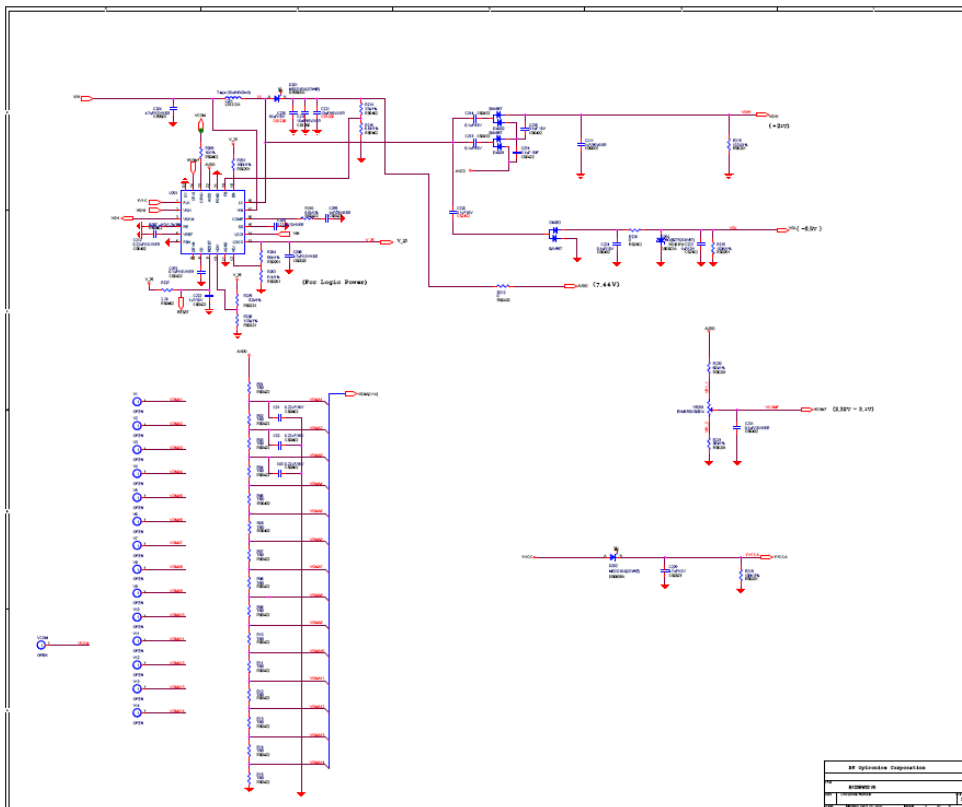
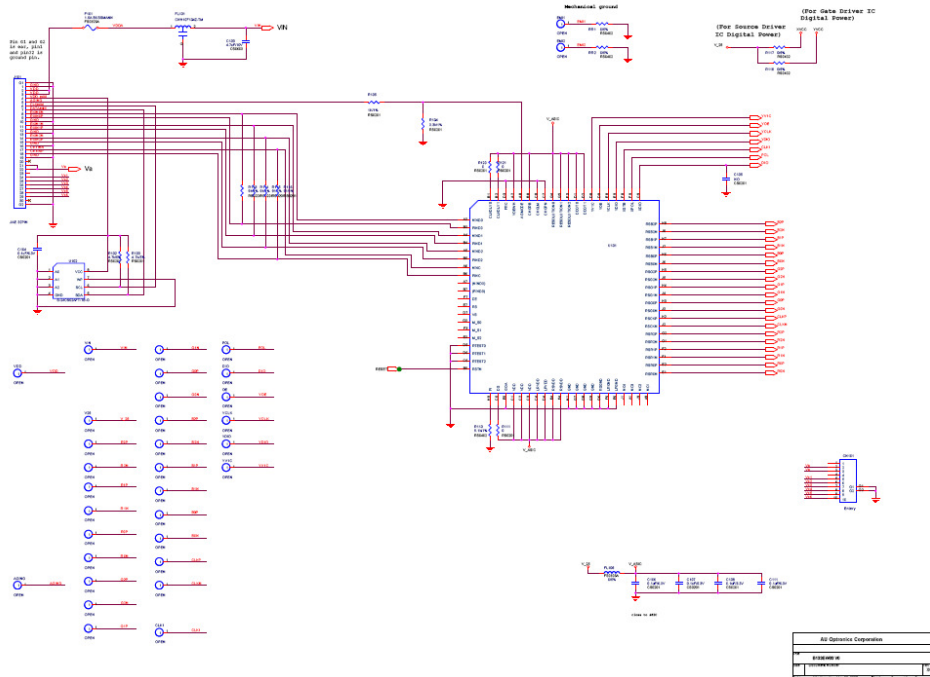
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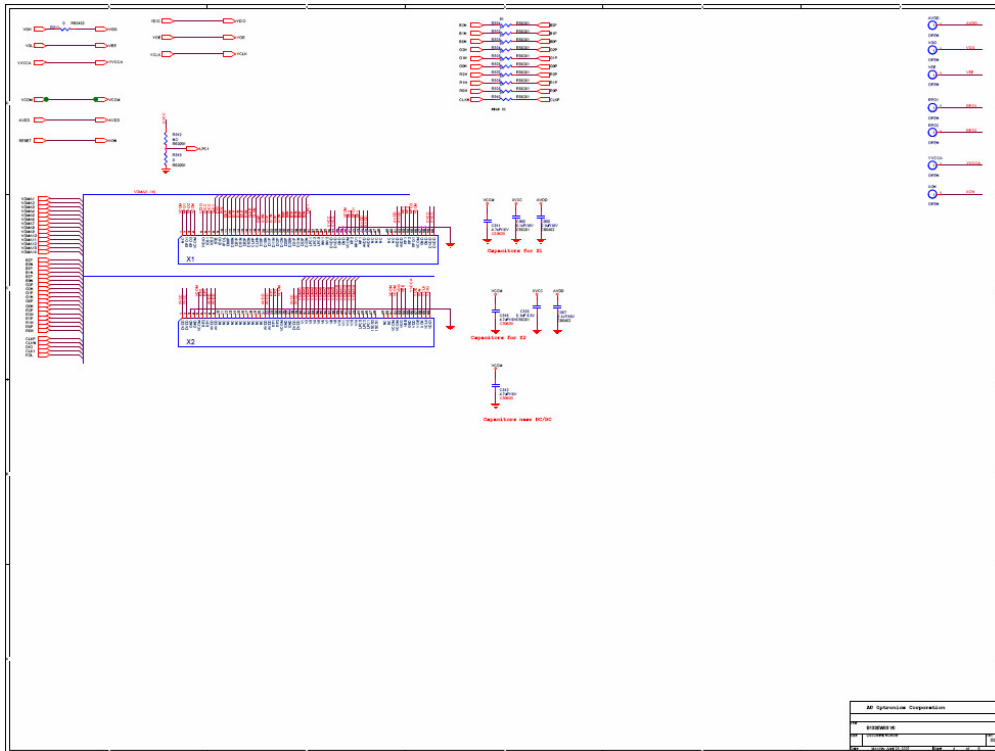
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## 4.6. Display PCB Schematics





#### 4.7. Display PCB Layout

#### Display Subsystem (PCB & TFT Panel)

##### 4.7.1. Pin-Out (Single Channel LVDS Interface)

Connector: **IPEX 20474-030E-12** or equivalent (1.0 mm thickness, lock-in type, pin 1 starts from left on the front)

Matching Connector: **IPEX 20472-030T-10** or equivalent (micro-coax type)

Interface Chips: (need update according the latest Configuration Sheet), integrated LVDS and timing controller)

Single Channel LVDS Configuration			
Pin	Symbol	Description	Micro-coax cable gauge (AWG)
1	GND	Ground	40
2	V <sub>cc</sub>	Power Supply (+3.3V)	36
3	V <sub>analog</sub>	Power Supply (+3.3V)	36
4	V <sub>EDID</sub>	DDC Power +3.3V	40

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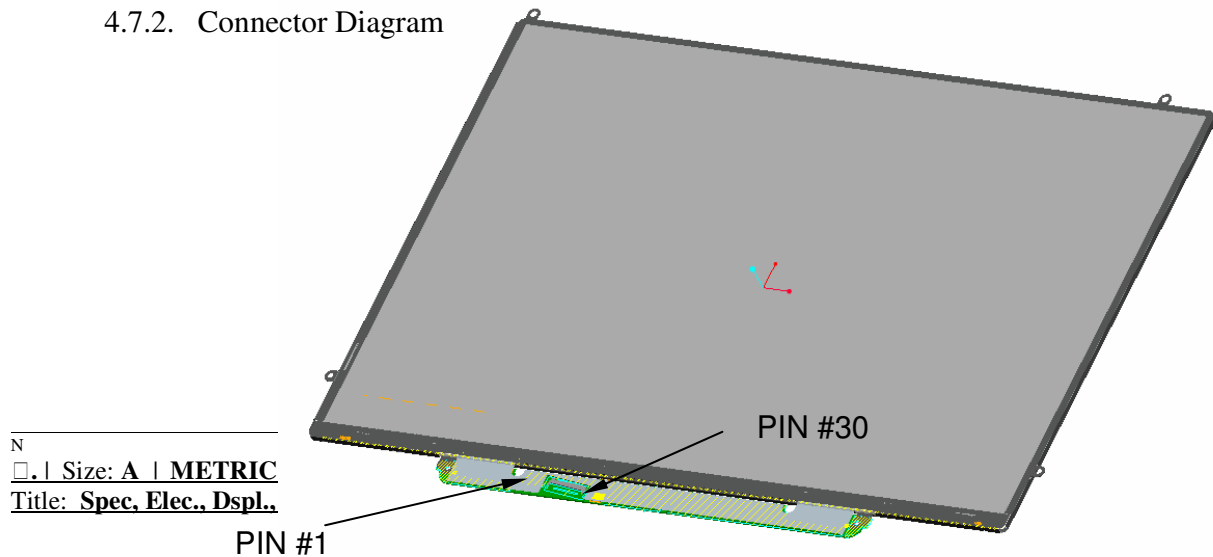
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5	Vsync	Vsync	40
6	Clk <sub>EDID</sub>	DDC Clock	40
7	DATA <sub>EDID</sub>	DDC Data	40
8	Rin0-	Differential Data Input	40
9	Rin0+	Differential Data Input	40
10	GND	Ground	40
11	Rin1-	Differential Data Input	40
12	Rin1+	Differential Data Input	40
13	GND	Ground	40
14	Rin2-	Differential Data Input	40
15	Rin2+	Differential Data Input	40
16	GND	Ground	40
17	Clkin-	Differential Clock Input	40
18	Clkin+	Differential Clock Input	40
19	GND	Ground	40
20	NC	NC	40
21	Vdc(1 &2)	LED Annode (Positive)	40
22	Vdc(3&4)	LED Annode (Positive)	40
23	NC	NC	40
24	Vdc1	LED Cathode (Negative)	40
25	Vdc2	LED Cathode (Negative)	40
26	Vdc3	LED Cathode (Negative)	40
27	Vdc4	LED Cathode (Negative)	40
28	Vdc5	LED Cathode (Negative)	40
29	Vdc6	LED Cathode (Negative)	40
30	NC	NC	40

#### 4.7.2. Connector Diagram



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### 4.7.3. Color Input Data Reference

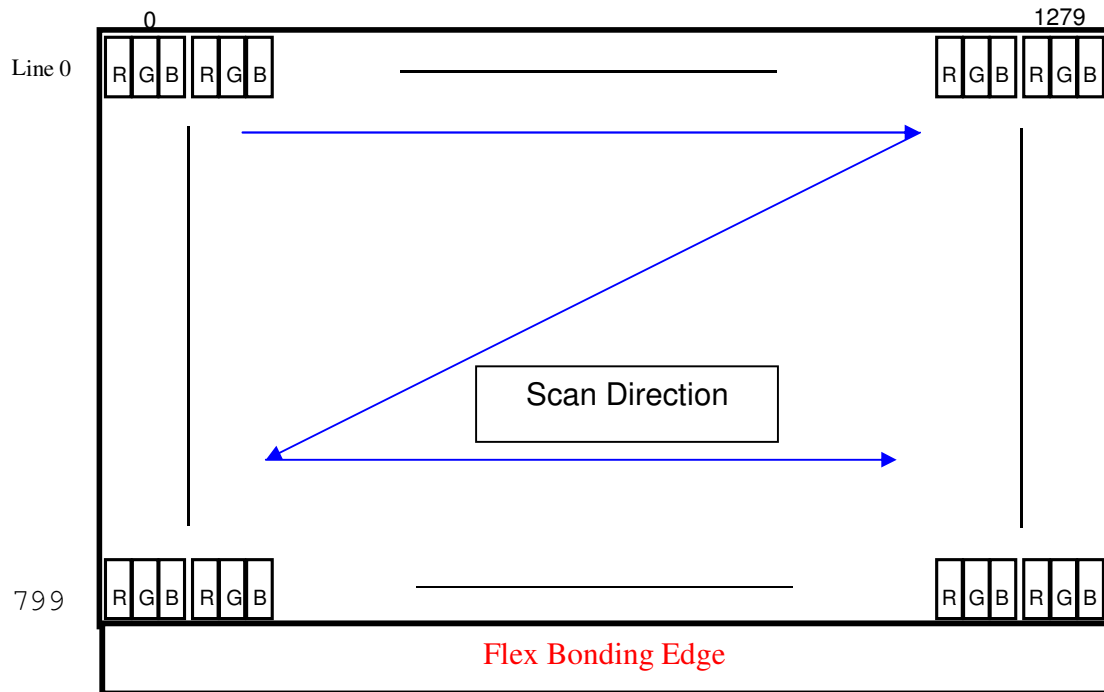
The brightness of each primary color (red, green and blue) is based on the 6-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides a reference for color versus data input.

COLOR DATA REFERENCE

Color		Input Color Data																	
		Red						Green						Blue					
		MSB			LSB			MSB			LSB			MSB			LSB		
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green(63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue(63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red	Red(00) Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(01)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(02)	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red(61)	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(62)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(63) Bright	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Green	Green(00)Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(01)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	Green(02)	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green(61)	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	0
	Green(62)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
	Green(63)Bright	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0

Blue	Blue(00) Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(01)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(02)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(61)	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1
	Blue(62)	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
	Blue(63) Bright	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

Pixel Format on the Display





4.7.4. EDID Interface (Per Vesa EDID 1.x standard requirements)

2	B133EW07	Value	Value	Note
Header	HEX	BIN	DEC	
	00	00000000	0	
	FF	11111111	255	
	FF	11111111	255	
	FF	11111111	255	
	FF	11111111	255	
	FF	11111111	255	
	FF	11111111	255	
EISA Manuf. Code LSB	00	00000000	0	
Compressed ASCII	06	00000110	6	<b>APP9CC2</b>
Product Code	10	00010000	16	<b>0 00001(A) 10000(P) 10000(P)</b>
hex, LSB first	C2	11000010	194	<b>9CC2 (apple assigned code)</b>
32-bit ser #	9C	10011100	156	
	01	00000001	1	<b>unused</b>
	01	00000001	1	
	01	00000001	1	
	01	00000001	1	
Week of manufacture	01	00000001	1	<b>Week 1</b>
Year of manufacture	13	00010011	19	<b>19(2009-1990=19)</b>
EDID Structure Ver.	01	00000001	1	
EDID revision #	03	00000011	3	
Video input definition	80	10000000	128	<b>Digital Input</b>
Max H image size	1D	00011101	29	<b>28.6cm</b>
Max V image size	12	00010010	18	<b>17.9cm</b>
Display Gamma	78	01111000	120	<b>Gamma 2.2</b>
Feature support	0A	00001010	10	<b>no DPMS,Active off,RGB color</b>
Red/green low bits	C5	11000101	197	
Blue/white low bits	95	10010101	149	
Red x/ high bits	A3	10100011	163	<b>Rx=0.640</b>
Red y	57	01010111	87	<b>Ry=0.340</b>
Green x	4F	01001111	79	<b>Gx=0.310</b>
Green y	9C	10011100	156	<b>Gy=0.610</b>
Blue x	26	00100110	38	<b>Bx=0.150</b>
Blue y	0F	00001111	15	<b>By=0.060</b>
White x	50	01010000	80	<b>Wx=0.313</b>

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<b>White y</b>	54	01010100	84	Wy=0.329
Established timing 1	00	00000000	0	unused
Established timing 2	00	00000000	0	
Manufacturer's Timing	00	00000000	0	
Standard timing #1	01	00000001	1	unused
	01	00000001	1	
Standard timing #2	01	00000001	1	
	01	00000001	1	
Standard timing #3	01	00000001	1	
	01	00000001	1	
Standard timing #4	01	00000001	1	
	01	00000001	1	
Standard timing #5	01	00000001	1	
	01	00000001	1	
Standard timing #6	01	00000001	1	
	01	00000001	1	
Standard timing #7	01	00000001	1	
	01	00000001	1	
Standard timing #8	01	00000001	1	
	01	00000001	1	
Pixel Clock/10,000 (LSB)	52	01010010	82	<b>Timing Descriptor #1</b> 1280x800 @60_mode:pixel clock=72.5MHz
Pixel Clock/10,000 (MSB)	1C	00011100	28	
Horiz. Active pixels(Lower 8 bits)	00	00000000	0	Horiz active=1280 pixels
Horiz.Blanking (Lower 8 bits)	8F	10001111	143	Horiz blanking=143pixels
Horiz. Active pixels:Horiz. Blanking (Upper4:4 bits)	50	01010000	80	Vertical active=800 lines
	20	00100000	32	
	2E	00101110	46	Vertical blanking=46 lines
Vert. Active pixels:Vert. Blanking (Upper4:4 bits)	30	00110000	48	Horiz sync. Offset=48 pixels
	30	00110000	48	
	20	00100000	32	Horiz sync. Pulse Width=32 pixels
Vert. Sync. Offset=xx lines, Sync Width=xx lines	36	00110110	54	Verti sync. Offset=3 lines, Sync Width=6 lines
Horiz. Ver. Sync/Width (upper 2 bits)	00	00000000	0	
Hori. Image size (Lower 8 bits)	1E	00011110	30	Hori image size= 286 mm
Vert. Image size (Lower 8 bits)	B3	10110011	179	Verti image size = 179mm
Hori. Image size : Vert. Image size (Upper 4 bits)	10	00010000	16	
	00	00000000	0	Horizontal Border = 0

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	00	00000000	0	Vertical Border = 0
	18	00011000	24	
Detailed timing/monitor descriptor #2	00	00000000	0	
	00	00000000	0	
	00	00000000	0	
Version	01	00000001	1	For apple
Apple edid signature	00	00000000	0	For apple
Apple edid signature	06	00000110	6	For apple
Link Type (LVDS Link,MSB justified)	10	00010000	16	For apple
Pixel and link component format (6-bit panel interface)	20	00100000	32	For apple
Panel features (No inverter)	00	00000000	0	For apple
	00	00000000	0	For apple
	00	00000000	0	
	00	00000000	0	
	00	00000000	0	
	00	00000000	0	
	00	00000000	0	
	00	00000000	0	
	0A	00001010	10	
	20	00100000	32	
Detailed timing/monitor descriptor #3	00	00000000	0	ASCII Data String:B133EW07 V1
	00	00000000	0	
	00	00000000	0	
	FE	11111110	254	
	00	00000000	0	
	42	01000010	66	B
	31	00110001	49	1
	33	00110011	51	3
	33	00110011	51	3
	45	01000101	69	E
	57	01010111	87	W
	30	00110000	48	0
	37	00110111	55	7
	20	00100000	32	
	56	01010110	86	V
	31	00110001	49	1
	0A	00001010	10	

N

□. | Size: A | METRIC | Scale: NONE |

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Detailed timing/monitor descriptor #4	20	00100000	32	Monitor Name: Color LCD
	00	00000000	0	
	00	00000000	0	
	00	00000000	0	
	FE	11111110	254	
	00	00000000	0	
	43	01000011	67	
	6F	01101111	111	
	6C	01101100	108	
	6F	01101111	111	
	72	01110010	114	
	20	00100000	32	
	4C	01001100	76	
	43	01000011	67	
	44	01000100	68	
	0A	00001010	10	
	20	00100000	32	
	20	00100000	32	
	20	00100000	32	
Extension Flag	00	00000000	0	
Checksum	6D	01101101	109	
SUM			6400	

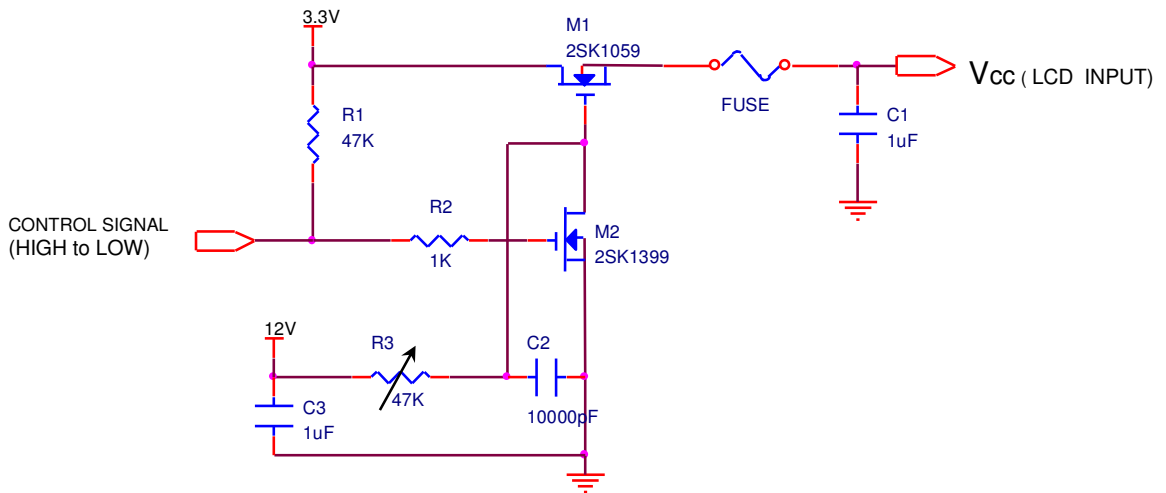
#### 4.7.5. Electrical Ratings

PARAMETER	SYMBOL	VALUES			UNIT	NOTES
		Min.	Typ.	Max.		
Power Supply Input Voltage	V <sub>CC</sub>	3.0	3.3	3.6	V (DC)	
Power Supply Ripple			50		mV <sub>p-p</sub>	1

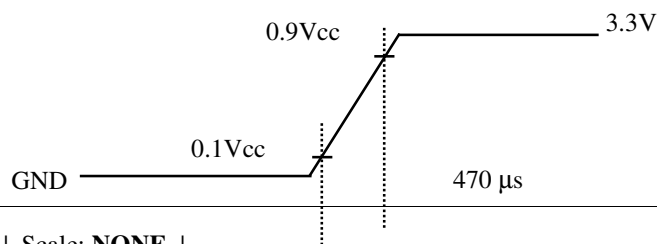
N

Power Supply Input Current	$I_{CC}$	-	242	273	mA	2
Differential Impedance	$Z_m$	90	100	110	$\Omega$	3
Power Consumption	$P_c$	-	0.8	0.9	W	2
Rush current	$I_{RUSH}$	-	-	1.5	A	4

- Notes: (1) The power supply ripple is measured whereas a black pattern is displayed;  
(2) The specified current and power consumption are under the conditions at  $V_{cc} = 3.3\text{ V}$ ,  $T = 25^\circ\text{C}$ , and  $f_v = 60\text{ Hz}$ ,  $f_{CLK}=72.5\text{MHz}$ , whereas a mosaic pattern (typical) is displayed;  
(3) This impedance value is needed to a proper display and is measured from LVDS mating connector to LVDS Rx  
(4) The following is a typical  $V_{cc}$  circuit on the system side



$V_{cc}$  rise time is about  $470\ \mu\text{s}$



N

□. | Size: A | METRIC | Scale: NONE |

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The duration of the rush current is about 20 ms.

#### 4.7.6. Signal Timing

##### 4.7.6.1. Signal Impedance

Defined in VESA standard for LVDS FPDI 2

##### 4.7.6.2. Timing Data

This is the signal timing required at the input of the control ASIC concerned with LVDS as a FlatLink or equivalent. All of the interface signal timing should be satisfied with the following specifications based on the VESA timing guideline (1280x800 @ 60 Hz) for its proper operation.

## Video Timing Data

Signal	Parameter	Symbol	Min	Typ	Max	Unit	Note
D <sub>CLK</sub>	Clock Period	T <sub>C</sub>		13.79		ns	1
	Clock Frequency	f <sub>C</sub>		72.50		MHz	1/T <sub>C</sub>
	Duty Ratio (% High)	K <sub>dr</sub>	40	50	60	%	T <sub>Ch</sub> /T <sub>C</sub>
	Rise Time	T <sub>RCLK</sub>	-	4.42	-	ns	
	Fall Time	T <sub>FCLK</sub>	-	4.42	-	ns	
DE (Data Enable Only) (DTMG) Data	DE Setup Time	T <sub>se</sub>	4	-	-	ns	2  f <sub>V</sub> =59.94 Hz, 3
	Data Setup Time	T <sub>sd</sub>	4	-	-	ns	
	Data Hold Time	T <sub>hd</sub>	2	-	-	ns	
	Horizontal Period	T <sub>H</sub>		1440		T <sub>C</sub>	
	Horizontal Blank Period	T <sub>ha</sub>		160		T <sub>C</sub>	
	Vertical Period	T <sub>V</sub>		823		T <sub>H</sub>	
H <sub>sync</sub>	H <sub>sync</sub> Back Porch	H <sub>bp</sub>		80		T <sub>C</sub>	Display Period
	H <sub>sync</sub> Pulse Width	T <sub>WH</sub>		32		T <sub>C</sub>	
	H <sub>sync</sub> Front Porch	H <sub>fp</sub>		48		T <sub>C</sub>	
	Horizontal Active Period	T <sub>HD</sub>	1280	1280	1280	T <sub>C</sub>	
V <sub>sync</sub>	V <sub>sync</sub> Back Porch	V <sub>bp</sub>		14		T <sub>H</sub>	Display Period
	V <sub>sync</sub> Pulse Width	T <sub>WV</sub>		6		T <sub>H</sub>	
	V <sub>sync</sub> Front Porch	V <sub>fp</sub>		3		T <sub>H</sub>	
	Vertical Active Period	T <sub>VD</sub>	800	800	800	T <sub>H</sub>	

- Note: (1) When the WXGA+ controller sets DE Mode, and H<sub>sync</sub> and V<sub>sync</sub> are required. The duration of DE (DTMG) signal must be longer than 1 clock period (T<sub>C</sub>) at every horizontal sync period;
- (2) Horizontal Period = One Line Scanning Time;
- (3) The vertical period T<sub>V</sub> is related to the frame frequency f<sub>V</sub>, i.e., 60 Hz.

### 4.7.6.3. Video Timing Diagram

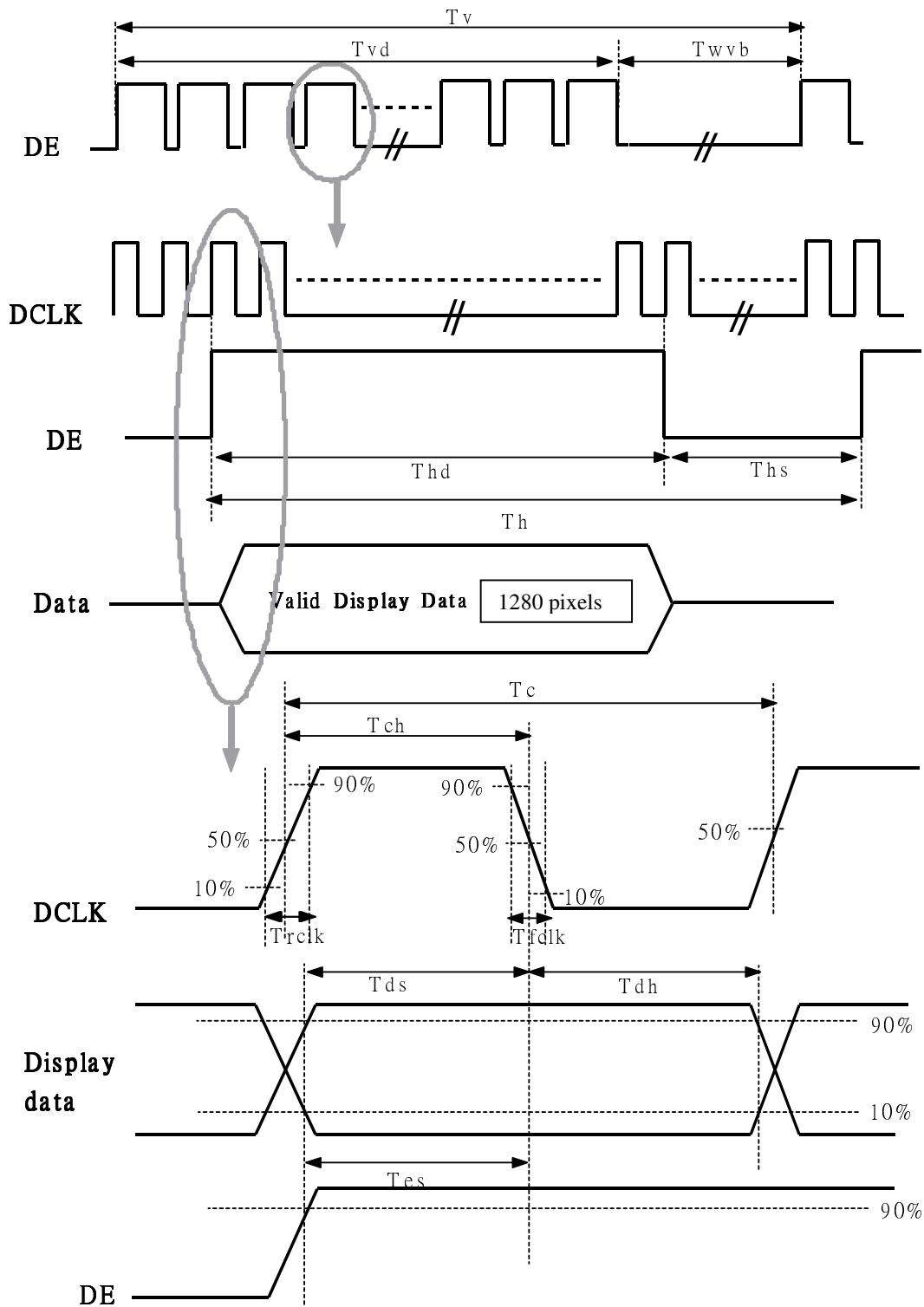
N

□. | Size: A | METRIC | Scale: NONE |

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□. | Size: A | METRIC | Scale: NONE |



#### 4.7.7. Power Measurements (W/O backlight)

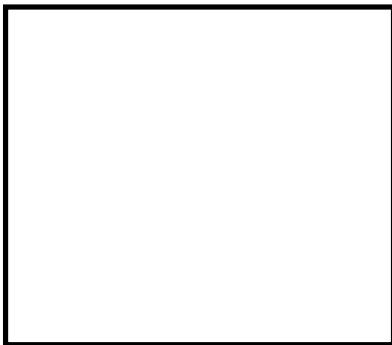
Pattern	Min	Typ	Max	Unit
White	To be updated			mA
Mosaic		242	273	mA
V. Stripe	To be updated			mA
Black		273	303	mA

Note: (1) Display data pins and timing signal pins should be connected (GND = 0V);

(2) Operation conditions:  $f_V = 60$  Hz,  $f_{CLK} = 72.5$  MHz,  $V_{CC} = 3.3$  V;

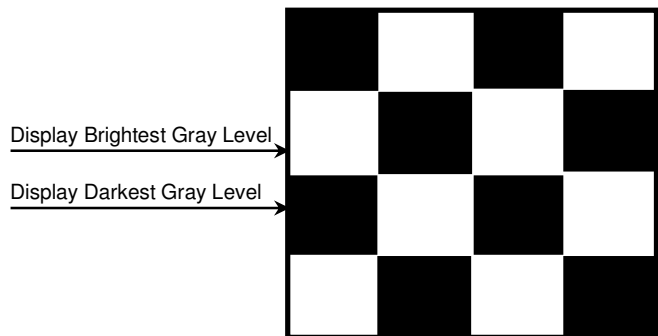
(3) Power dissipation patterns are as follows.

(a) White screen



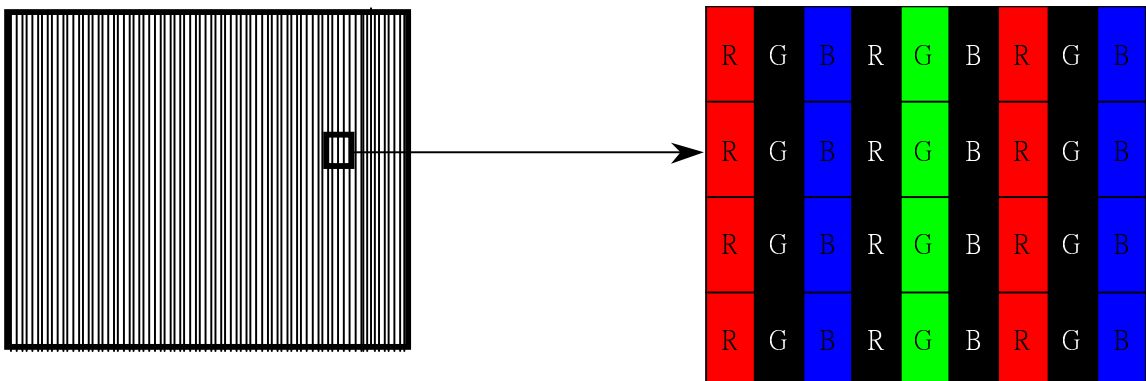
(b) Mosaic (or checker) pattern

*20x20 pixel black and white boxes*



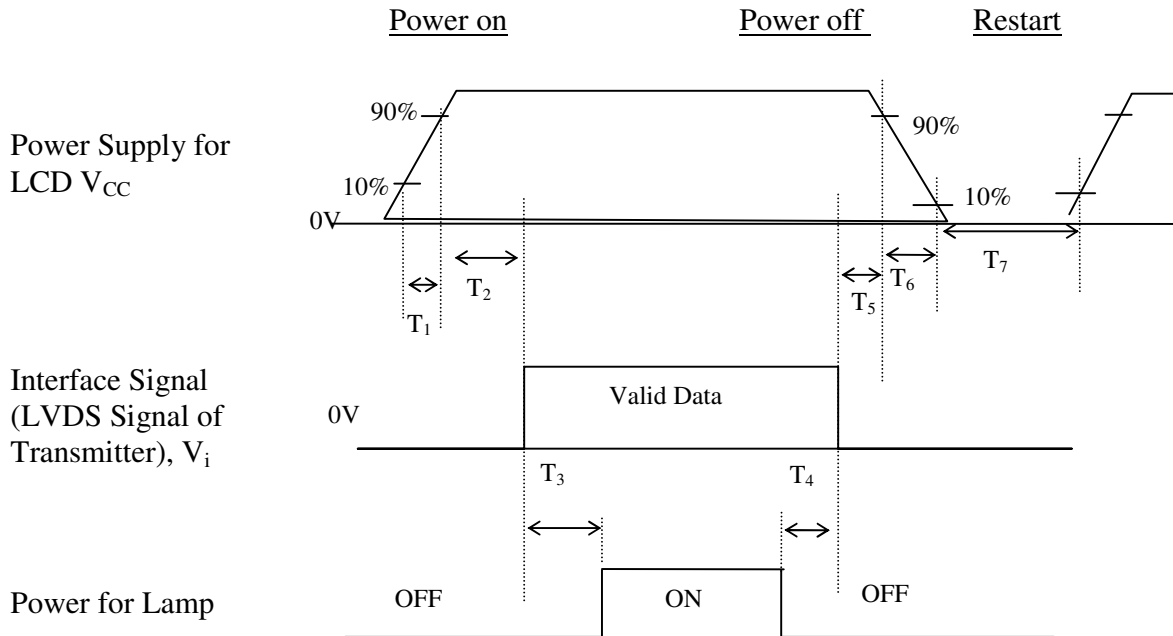
(c) Vertical Stripe Pattern

*sub-pixel vertical line on/off alternation,*



#### 4.7.8. Power on-off sequence

Power-on includes both system starting from power-off state and wake from sleep state; power-off includes both system shutdown and entering sleep state.



Parameter	Values			Unit
	Min.	Typ.	Max.	
T <sub>1</sub>	0.15	-	10	ms
T <sub>2</sub>	1	20	50	ms
T <sub>3</sub>	200	250	-	ms
T <sub>4</sub>	200	250	-	ms
T <sub>5</sub>	0	20	50	ms
T <sub>6</sub>	5	-	20	ms
T <sub>7</sub>	500	-	-	ms

#### 4.7.9. V<sub>cc</sub> Dip Condition

The V<sub>cc</sub> dip is the V<sub>cc</sub> voltage drop during panel start-up.

N

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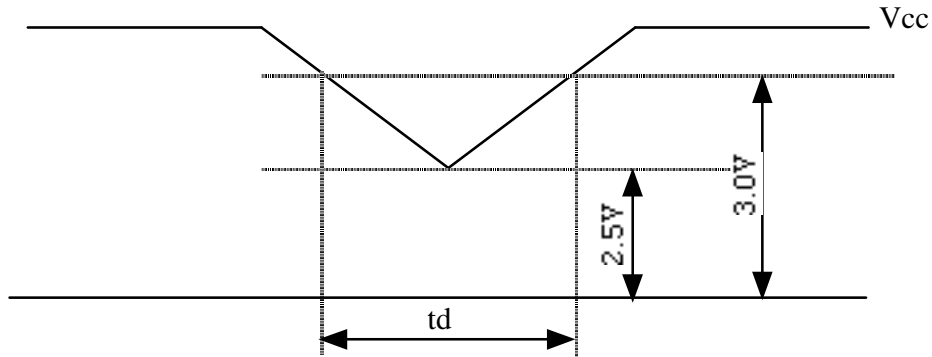
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(1)  $2.5V \leq V_{cc} < 3.0V$ ,  $T_d \leq 20$  ms;

(2) For  $V_{cc} < 2.5V$ ,  $V_{cc}$  should follow the power on-off sequence defined in 4.7.8



#### 4.8. Near-Field Noise

The RF emissions from the panel (especially the LVDS input and Tcon) interfere with Wifi operation.

Note that this spec compliance requirement is in addition to the legal EMI compliance requirements.

#### 4.9. Backlight Subsystem

##### 4.9.1. General Information

LED Manufacturer	Nichia
LED Manufacturer Assembly P/N	Nichia NNSW208
Number of LEDs	54
LED Ranks	V630 and up
LED Brightness Bin	50 mcd per bin
LED Vf Bin	Rank 1 (2.8-3.0 V) and 2 (3.0-3.2 V)
LED Forward Voltage Range for All 6 LED Series Lines	MAX: 28.8 V (Characterized at LVDS Connector for 23 mA)

##### 4.9.2. Backlight Synchronization Requirement (to avoid BL shimmering)

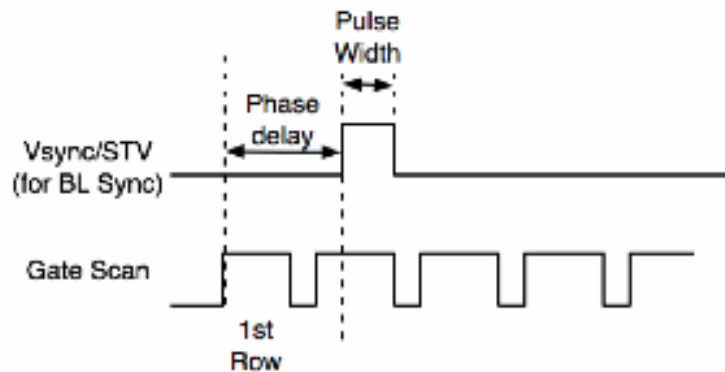
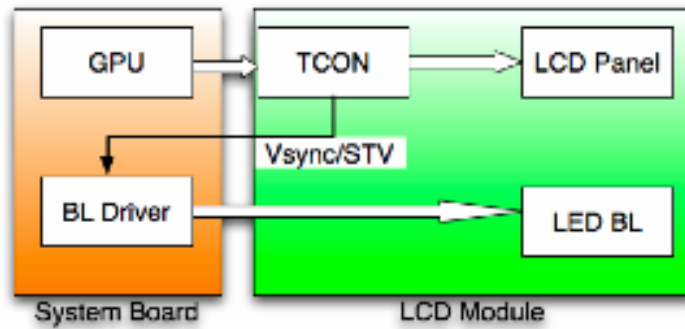
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□. | Size: A | METRIC | Scale: NONE |

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The Vsync/STV signal is a once-per-frame pulse that has a constant phase delay with respect to the start of the frame. This signal is used by the backlight LED driver to synchronize BL PWM with the frame update to avoid shimmering (waterfall) artifacts in the image.

The minimum pulse width is 1 us.

#### 4.9.3. Backlight Electrical Characteristics

The backlight brightness test shall be tested at 600Hz PWM 94% cycle & 23 mA peak current with following percentage duty cycle

LED Current (% duty cycle)	LED Forward Voltage for any LED string	Power (W) Assuming 3.2V max forward bias	Display Minimum Luminance (nits)	Display Typical Luminance (nits)	Display Maximum Luminance (nits)
94%	28.8 V	3.73	250	275	300

N

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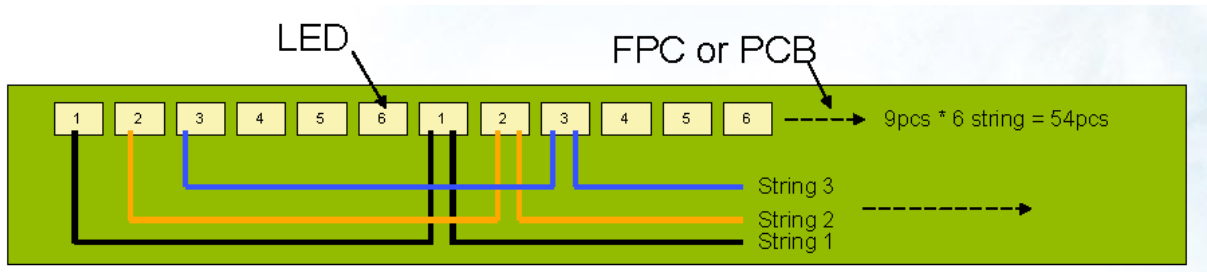
Title: Spec, Elec., Dspl., AUO, 13.3" TFT-LCD

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19%	28.8 V	0.75	50	55	60
5%	28.8 V	0.19	12	14	15

#### 4.9.4. LED Connection

String	LED1	LED2	LED3	LED4	LED5	LED6	LED7	LED8	LED9
1	1	7	13	19	25	31	37	43	49
2	2	8	14	20	26	32	38	44	50
3	3	9	15	21	27	33	39	45	51
4	4	10	16	22	28	34	40	46	52
5	5	11	17	23	29	35	41	47	53
6	6	12	18	24	30	36	42	48	54



## 5. OPTICAL REQUIREMENTS

### 5.1. Optical Specifications

Supplier must submit optical measurement data from 20 samples for items marked critical in Table 6.1.1. The optical performance will be based on supplier's measurement data, visual inspection of the samples, verification measurements, and specification correlation.

**Table 6.1.1: Optical Characteristics**

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Iso-Contrast Viewing Angle CR ≥ 10	θ	up	45	50	--	Degrees	1,2,3
		down	45	50			
		left/right	55/55	60/60			
Contrast ratio	CR	Optimal	400	600	--	--	1,2,3
Luminance	Y	I <sub>LED</sub> =23 mA @94% duty cycle	220	250	--	cd/m <sup>2</sup>	1,2,4
Global Luminance Uniformity		Optimal	50		--	%	1,2
Worst Neighbor Luminance Uniformity		Optimal	80		--	%	1,2
Gamma	γ	--	--	2.2	--	--	1,2,3
Flicker	F	No Visual Flicker	--	--	-30	dB	1,2,3
Cross Talk	D <sub>SHA</sub>	Optimal	--		2.0	%	1,2,3
Worst Low Level (dark) Inversion Viewing Direction		PCB on the bottom	--	6:00	--	o'clock	1,2
Response (rise+fall time)	τ <sub>on+off</sub>	θ = 0°, Ta=25°C	--	16	25	ms	1,2,3
Gray to Gray Response time	τ <sub>G2G</sub>	θ = 0°, Ta=25°C	--		40	ms	1,2,3
White Chromaticity (all panels)	x	CIE 1931	0.297	0.313	0.329	--	1,2,3
	y		0.313	0.329	0.345	--	1,2,3
White Chromaticity (Within one panel)	delta x				0.005		
	delta y				0.008		
Red Chromaticity	x	CIE 1931	0.620	0.640	0.660	--	1,2,3
	y		0.315	0.330	0.345	--	1,2,3

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□. | Size: A | METRIC | Scale: NONE |

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Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Green Chromaticity	x	CIE 1931	0.290	0.310	0.330	--	1,2,3
	Y		0.590	0.610	0.630	--	1,2,3
Blue Chromaticity	X	CIE 1931	0.120	0.150	0.170	--	1,2,3
	Y		0.040	0.060	0.080	--	1,2,3
Max color difference within one panel	du'v'	white			0.005		1,2
Max color difference w.r.t. Center within one panel	du'v'	white			0.003		1,2
Max color difference from panel to panel	du'v'	white			0.008		
Max color difference between neighbors	du'v'	white			0.0025		1,2

Note 1: The testing conditions are specified in 6.2.

Note 2: The definitions of optical characteristics are shown in 6.3.

Note 3: Measured at center point. Equivalent performance over the entire panel required.

Note 4: Both center point and average of 160 points.

## 5.2. Measuring Conditions

The optical characteristics are determined after the unit has been 'ON' and stable for approximately 30 minutes at the maximum brightness, in a dark environment at an ambient temperature at  $25^{\circ}\text{C} \pm 2^{\circ}\text{C}$ . The electrical conditions include  $V_{cc} = 3.3 \text{ V}$ ,  $f_v = 60 \text{ Hz}$ ,  $f_{CLK} = 72.5 \text{ MHz}$ ,  $I_{BL} = 23 \text{ mA @94\%}$  duty cycle with 600Hz. Recommended measuring equipments for luminance and color are CCD based imaging systems such as Radiant Imaging Prometric 1400 system, or Colorimeter such as Photo Research PR650, TOPCON BM-5A or similar. The measuring distance should be about 50 cm from the LCD surface at normal unless otherwise specified. Measurements should be done on the 160 grid points as shown in the following figures. The measurement spot at the center is approximately 12 mm in diameter from a distance of 400 mm by TOPCON BM-5A or 15 mm in diameter from a distance of 500 mm by PR 650.

Viewing angle measurements should be done by an Eldim EZ Color system or similar.

N

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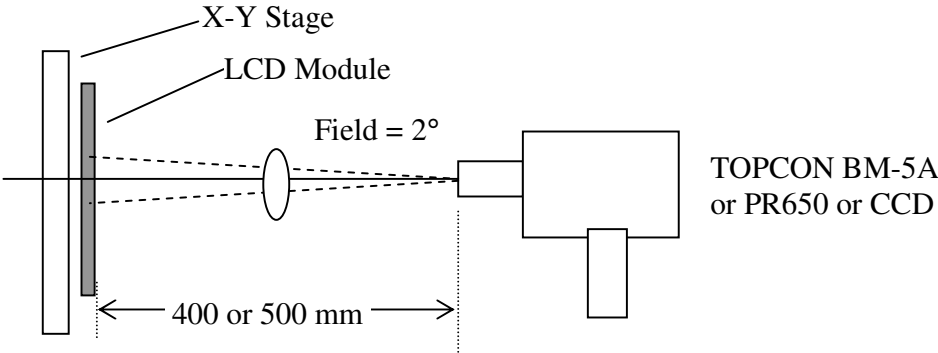
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The CIE 1931 or 1976 Standards will be used.

**Luminance and Color Measurement**



**Viewing Angle Measurement**

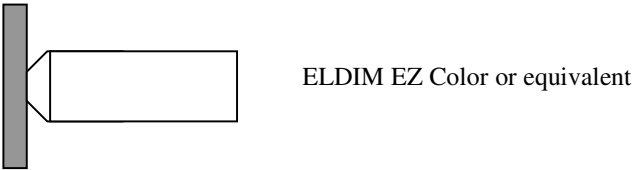


Figure 6-1: Optical Measurement Set-up



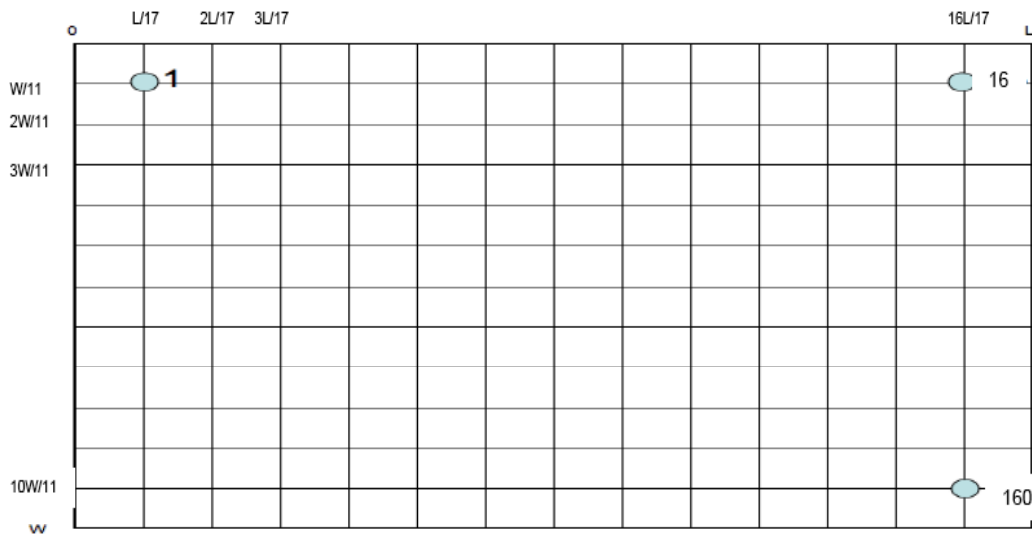


Figure 6-2: Measurement point location. L and W are the length and width of Active Area respectively.

### 5.3. Definition

#### 5.3.1. Center Point Luminance

$$L_{ct} = (L_{72} + L_{73} + L_{88} + L_{89}) / 4 \{ \text{Average Luminance value at point \#72, 73, 88, 89} \}$$

#### 5.3.2. Average Luminance

$$L_{Ave} = \text{SUM}(L_1 : L_{160}) / 160$$

where  $L_1$  to  $L_{160}$  are the luminance values measured at point #1 to #160.

#### 5.3.3. Luminance Uniformity

The entire display active area shall be scanned with the luminance measurement with white screen set full brightness.

two kinds of data for brightness uniformity: Luminance Uniformity, and Worst Neighbor Luminance Uniformity. The definitions are shown in below:

##### 5.3.3.1. Global Luminance Uniformity:

$$U = 100\% - (L_{max} - L_{min}) / L_{max}$$

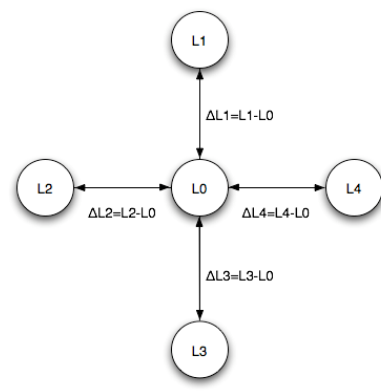
where,  $L_{max} = \max \{ \text{Luminance values at 160 points} \}$ ,

$$L_{\min} = \min \{ \text{Luminance values at 160 points} \}$$

5.3.3.2. Worst Neighbor Luminance Uniformity (The 4 points that are closest to the test point)

$$WNU = 100\% - \text{Max}(\Delta L1, \Delta L2, \Delta L3, \Delta L4) / L0$$

$$\text{Global WNU} = \min (WNU1, \dots WNU160)$$



5.3.4. Contrast Ratio

$$CR = \text{Luminance at } G_{\max} / \text{Luminance at } G_{\min} \{ \text{Average contrast value at point \#72, 73, 88, 89} \}$$

5.3.5. White Color Uniformity

The entire display active area shall be scanned with the color coordinate measurement with white screen set full brightness.

5.3.5.1. Panel to Panel White Color Uniformity

The center point (as defined by the average value at point #72, 73, 88, 89) white color coordinate of any panel shall be within the box with 4 corners coordination boundary listed in Table 6.1.

### 5.3.5.2. Max Color Difference with respect to the center within a panel

On each panel, the maximum color difference between any of the 160 points and the center point (defined as the average value at point #72, 73, 88, 89), represented in delta u'v'.

### 5.3.5.3. Max Color Difference between any two points within the panel

On each panel, the maximum color difference between any two of the 143 points, represented in delta u'v'.

### 5.3.5.4. Max Color Difference between two neighbors

On each panel, the maximum color difference between any two neighboring points on the panel, represented in delta u'v'.

### 5.3.6. RGB Color Chromaticity

The entire display active area shall be scanned with the color coordinate measurement with screen set to full brightness and solid R, G, B color respectively. The measured color coordinate of any panel shall be within the box with 4 corners coordination boundary listed in Table 6.1.

### 5.3.7. Viewing Angle

The viewing angle is defined as the viewing angle range under the condition at  $CR \geq 10:1$ .

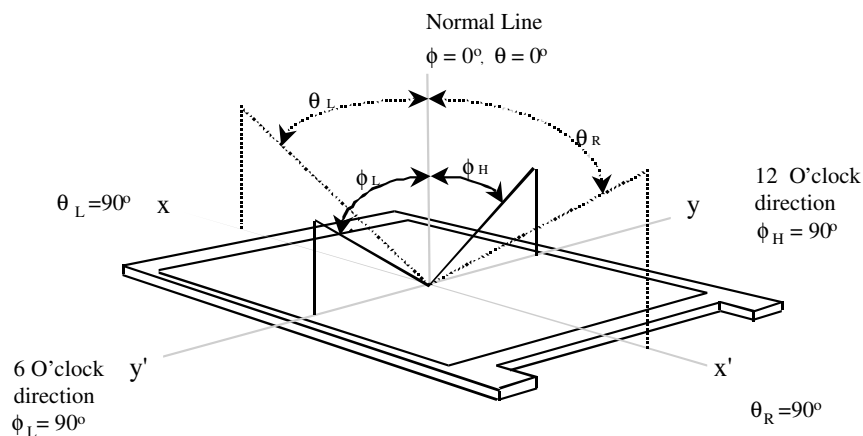


Figure 6-4: Viewing angle definition

5.3.8. Gray Scale Inversion

Luminance vs. viewing angle curves are measured based on gray level 255, 223, 191, 159, 127, 95, 63, 32 and 0, in the viewing angle of left, right, up, down, with PCB on the bottom side. Gray scale inversion happens when a higher gray scale measures the same luminance or lower luminance than any of the lower gray scale.

5.3.9. Response Time

5.3.9.1. On and Off Response Time

The On/Off response time,  $t_R + t_F$ , is defined in the following figure and shall be measured by switching the input signal for “black” and “white”.

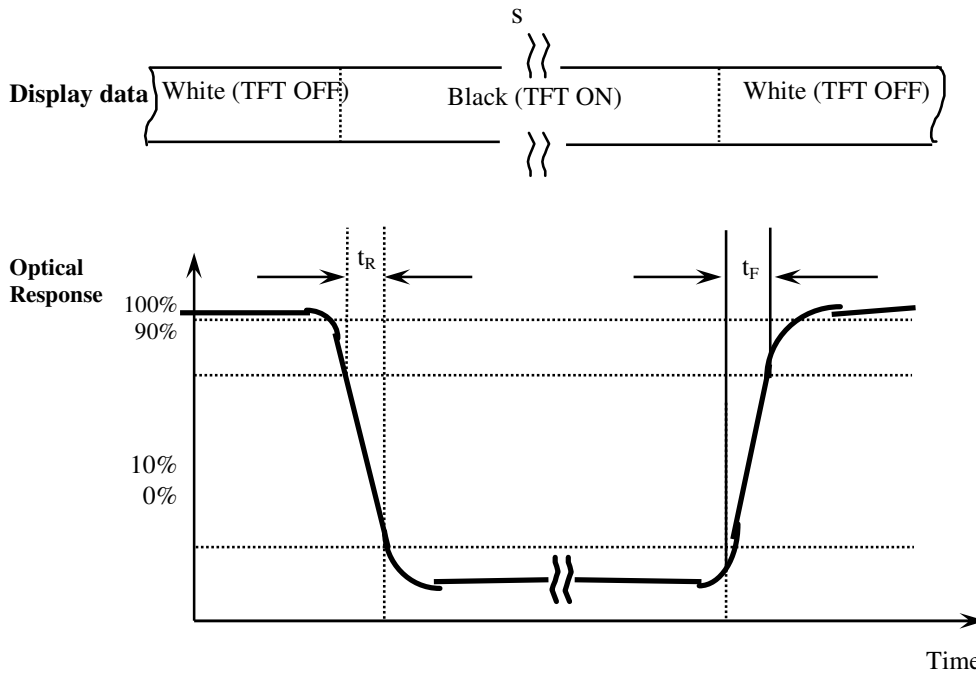


Figure 6-5: Response Time Measurement

5.3.9.2. Gray to Gray Response Time

Gray to Gray Response Time is measured in a similar method. But instead of switching display between black and white, panel is switched between two gray scales. The maximum gray-to-gray response time is based on 9 levels of gray

scales. The 9 levels are: gray level 255, 223, 191, 159, 127, 95, 63, 32 and 0. Figure 6-6 shows an example of Gray to Gray Response Time measurement data.

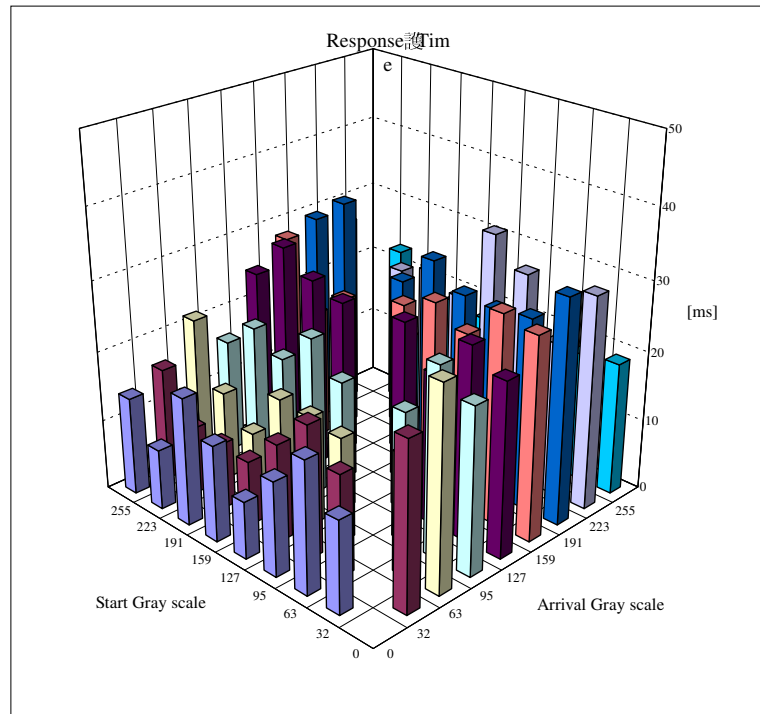


Figure 6-6: Gray to Gray Response Time

### 5.3.10. Gray Scale Linearity or Gamma Value

The display luminance,  $L_G$ , is measured at the different gray scales,  $G_{\min}$ , ...,  $G_{\max}$ . The exponential fitting is used to determine the gamma ( $\gamma$ ) value, which should be an intrinsic or uncorrected characteristic.

$$L_G \sim G^\gamma.$$

### 5.3.11. Flicker

**No visual flicker will be allowed.** The flicker level should be measured with either vertical stripes or a checker pattern, defined in Sec. 5.3.6. The output signal of a photometer is sent to an FFT analyzer. The flicker is essentially a ratio of the powers in the frequency spectrum at 30 Hz ( $P_x$ ) and 0 Hz ( $P_0$ ), *i.e.*,

$$F = 10 \text{ Log } (P_x / P_0).$$

#### 5.3.12. Cross-talk

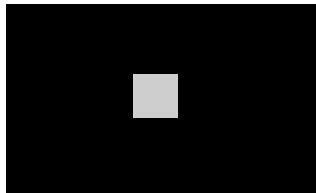
No visual cross-talk will be allowed. Two luminance values are measured at center spot with 50 x 50 pixels. The cross-talk,  $D_{SHA}$ , is defined as,

$$D_{SHA} = (L_B - L_A) / L_B \cdot 100\%,$$

Where,  $L_A$  = Luminance in Pattern A

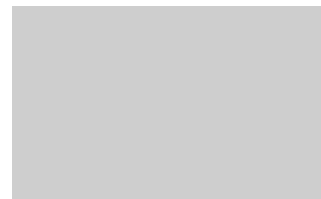
$L_B$  = Luminance in Pattern B.

Pattern A



Gray Scale = 127/255 in center  
Black in surrounding

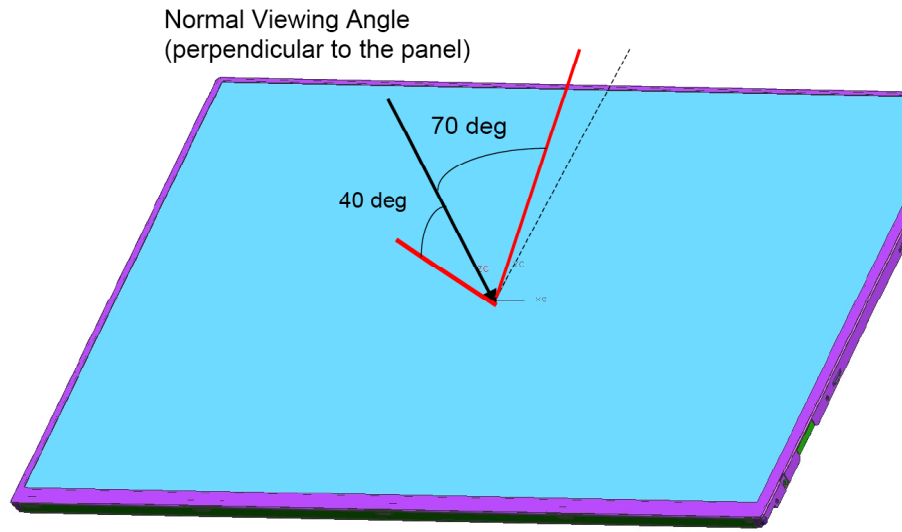
Pattern B



Gray Scale = 127/255 full screen

#### 5.4. Hot Spot Specifications:

The LED hot spot shall be inspected from 70 degree to -40 degree per the drawing below. There shall be no visible hot spot or no worse than “limited sample” hot spot (if there is a “limited sample” set up).



## 6. ENVIRONMENTAL

The display modules shall meet all functional and cosmetic specifications after testing to the environmental quality standards listed in this section. Additionally, the LCD modules in products shall pass all the system testing requirements listed in the end of this document.

### 6.1. Shock and Vibration

- 7.1.1 There will be no functional or cosmetic defects following a shock to all 6 sides delivering at least 200 G in a half sine pulse no longer than 2 ms to the display module, secured by its designated mounting details, in accordance with MIL-STD-202F Method 213B, test condition A.
- 7.1.2 There will be no functional defects following a shock delivering at least 260 g in a half sine pulse no longer than 2 ms to each of 6 sides. Each of the 6 sides will be shock tested with one each display, for a total of 6 displays. The displays are secured by designated mounting details, in accordance with MIL-STD-202F Method 213B, test condition A.
- 7.1.3 There will be no functional or cosmetic defects following a shock delivering at least 60 G in a pulse 11 msec or longer to the display module, secured by its designated mounting details, in accordance with MIL-STD-202F Method 213B, test condition A.
- 7.1.4 There shall be no functional or cosmetic defects following a vibration test, conducted at **3.0 G** from 5–150 Hz, 0.37 Oct/min with sine wave for 30 min./axis, with the display secured by its designated mounting details, and conducted in accordance with MIL-STD-202F, method 201A.

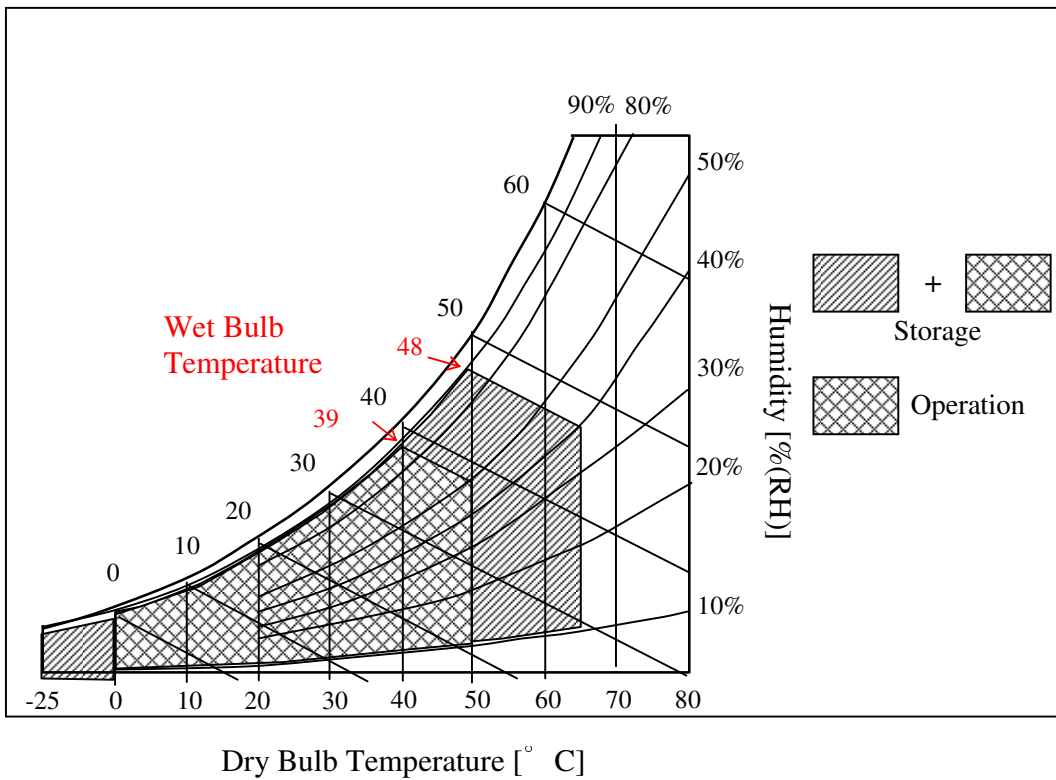


## 6.2. Temperature and Humidity

Unless otherwise stated in this specification, the display module must meet functional and cosmetic requirements after testing in accordance with Spec. # 080-0859, non-operating and operating conditions.

For these tests, the following limits set forth in Specification #080-0859 shall be altered to read.

### 6.2.1. General Performance Requirements



Note:

- 1) Maximum wet bulb temp operating temperature is 39° C.
- 2) Maximum wet bulb temp storage temperature is 48°C.

N

□. | Size: A | METRIC | Scale: NONE |

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## 6.2.2. Non-operational Testing

### 6.2.2.1. Low Temperature

-25°C @ 500 hrs

### 6.2.2.2. High Temperature

65°C @ 500 hrs

### 6.2.2.3. High Temperature and High Humidity

60°C @ 500 hrs, R.H. = 75% ± 10%

### 6.2.2.4. Thermal Shock

Cycle display from -25°C to 65°C with 5-minute transfer time,  
100 cycles at -25°C/65°C/-25°C.

## 6.2.3. Operational Testing

### 6.2.3.1. Low Temperature

0°C for 500 hours

### 6.2.3.2. High Temperature

50°C for 500 hours

### 6.2.3.3. High Temperature and High Humidity

50°C and 90% R.H. for 240 hours (Functional Check)  
Maximum wet-bulb temperature at 39°C or lower without  
condensation.

### 6.2.3.4. Four Corner Test (72 hrs – operating)

40°C @ 10% RH

40°C @ 90% RH

10°C @ 10% RH

10°C @ 90% RH

### 6.3. Altitude

72 hour storage

Operational: 15,000 Ft.

Non-Operational: 40,000 Ft.

## 7. RELIABILITY

### 7.1. Resistance to Normal Abuse

#### 7.1.1. Torsion Test

Module is fixed by 4 mounting holes (A, B, & C) on stable supports. Tester is connected to mounting hole on free floating module corner. Push/Pull test is conducted on all four corners.

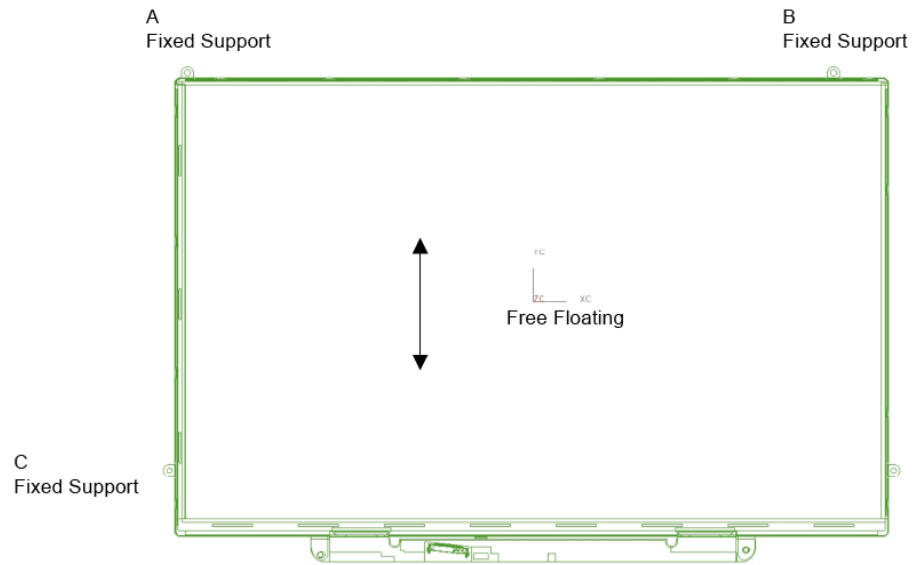
#### 7.1.2. Test Conditions:

Applied Force 20 N

Cycles 10 K

Frequency (F=push / pull) 1 Hz (1 cycle / sec.)

### 7.1.3. Test Set-up



### 7.1.4. Static Load Deflection and Breakage

Supplier shall demonstrate compliance per Specification 062-2208 Static Breakage Test

### 7.2. Electrostatic Discharge (ESD)

Display modules are to be tested for ESD susceptibility per specification 062-0302. The display modules must meet the Level 1 for the bare module, and Level 1 through III test requirements stated in the above referenced specification, when assembled in a portable computer.

### 7.3. MTBF

Supplier to demonstrate display module meets minimum 50,000 Hrs. @90% Confidence Supplier to include any acceleration factors included in the calculations. Power cycling frequency during this test is to be approved.

N

□. | Size: A | METRIC | Scale: NONE |

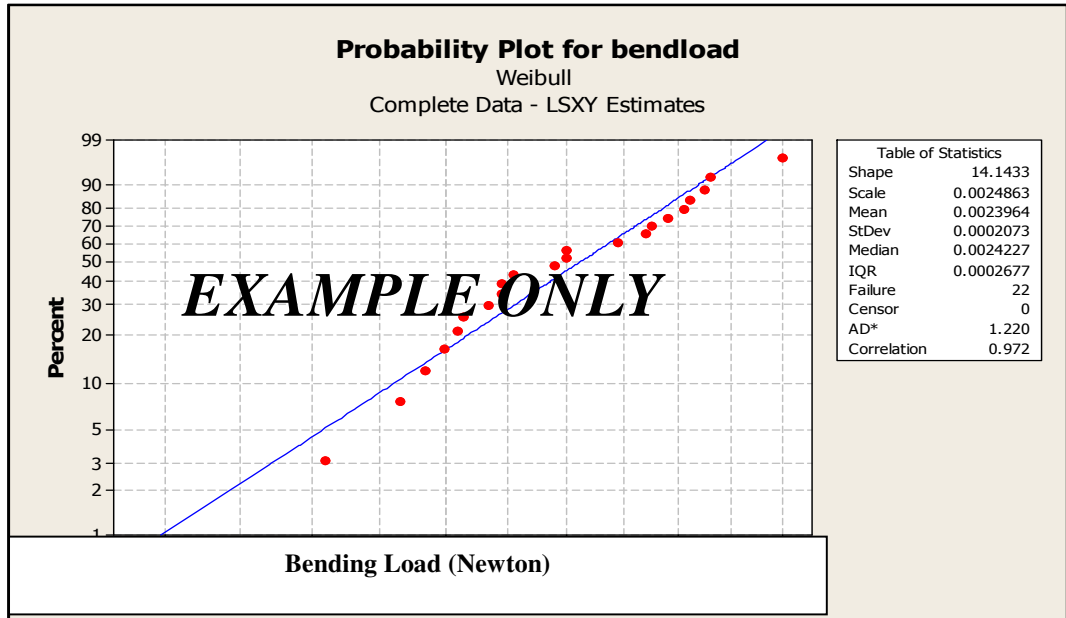
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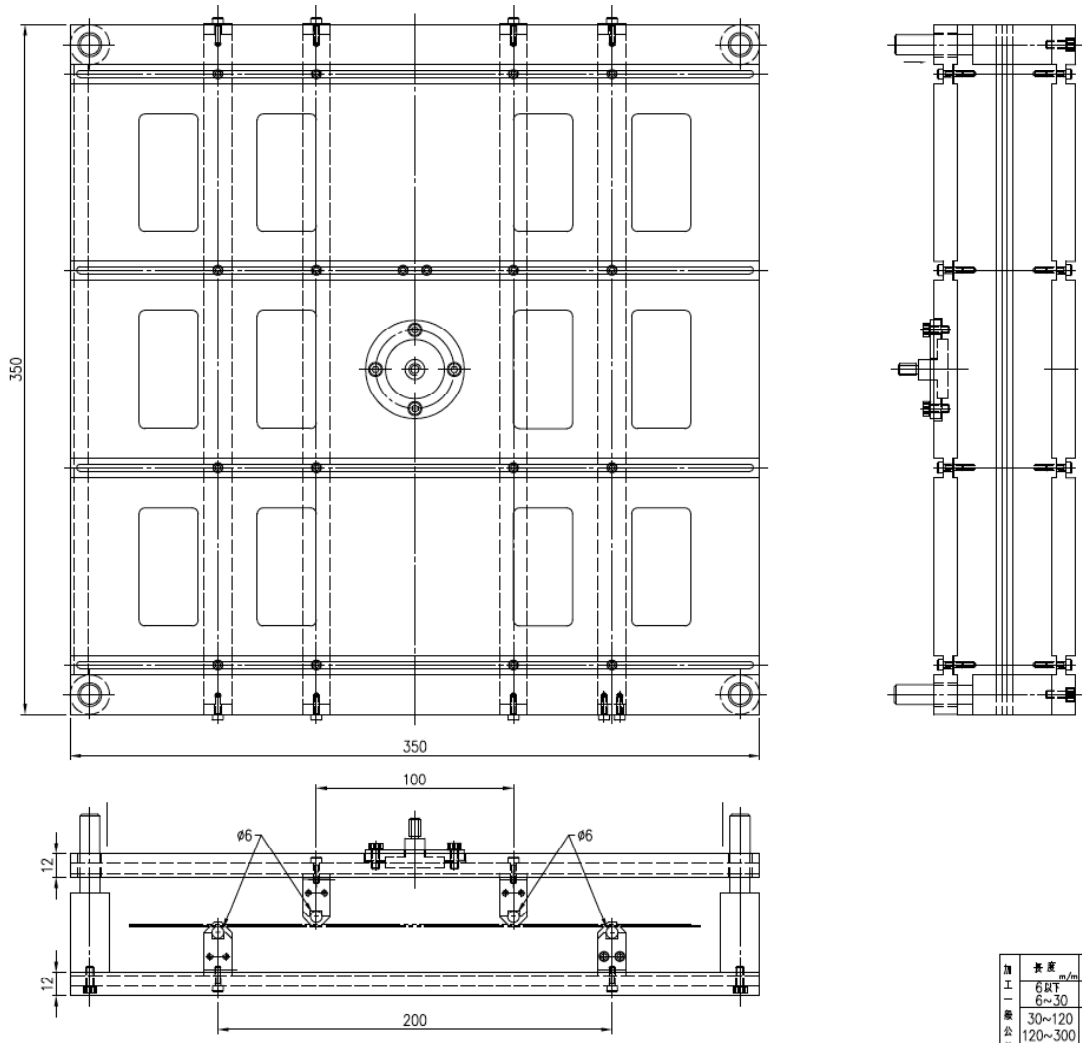
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## 7.4.LCD Glass Strength

The LCD glass strength (failure load) will be defined at a single 90% survival rate value on Weibull distribution. Please provide the optimized loading performance in the similar chart format below. The failure load of the 90% Weibull survival rate shall be higher than TBD N.



The 4 point bend test shall be used for the LCD glass strength test. The detailed fixture design/ shall follow the **ASTM standard C158-02**. The fixture is used in conduction with a load-displacement machine, commonly known as Instron.



Two orientations must be tested for this specification: orientation A (Figure 2.A) and orientation B (Figure 2.B)

This test shall be performed on 30 samples, **WITH current POLARIZERS** laminated on both top and bottom of the LCD glass, per applicable orientation as a First Article Inspection and when settings, tooling, and equipment are modified. Supplier is responsible for monitoring glass strength on an ongoing production basis. The test shall be conducted with a top rollers velocity of 1 mm/min. As soon as the first plane breaks, the test shall be stopped to prevent the second plane from breaking.

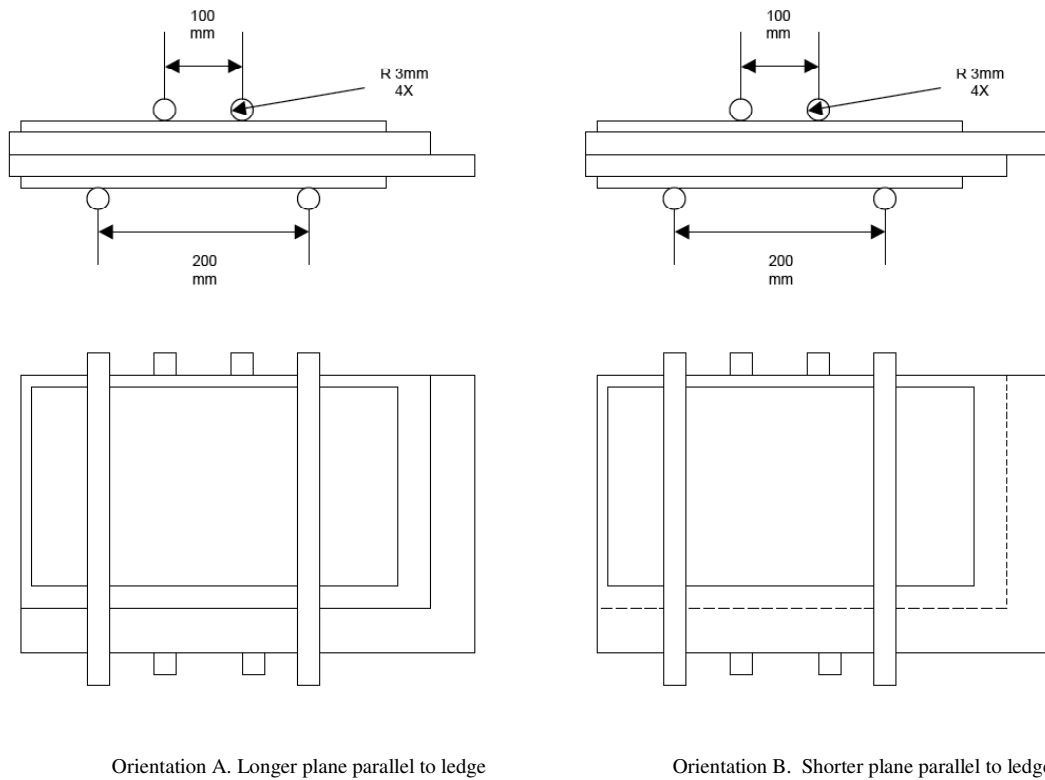


Figure 2. Display orientations measuring strength at edges

#### LCD glass strength data collection

Failure initiation site must be determined by visual inspection by selecting one of the different cases shown below (Figure 3).

Case A) If the failure is starting from the bottom edge or close to it, enter letter A.

Case B) If the failure is starting from the top edge or close to it, enter letter B.

Case C) If the failure is starting from the surface of glass, away from the edges and showing branching in both directions, enter letter C.

Case D) When testing in orientation D (Figure 1.D), if the failure is starting at the epoxy region between the panes, enter letter C edges of the glass (case D).

Case E) If during testing a snap is heard, but no crack is visible, enter letter E

Case O) If the failure does not match any of the above or cannot be easily recognized due to catastrophic breakage, enter letter O.

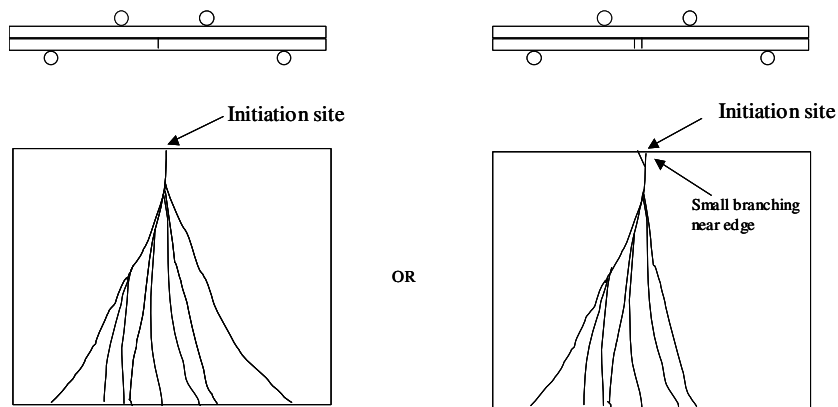
N

□. | Size: A | METRIC | Scale: NONE |

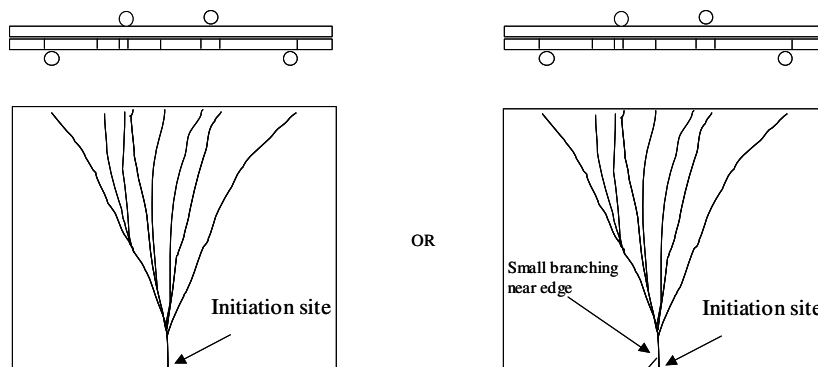
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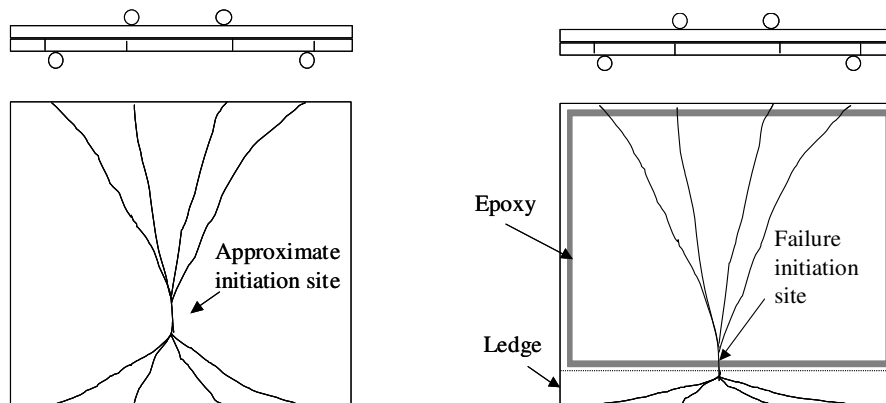
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Case A. Failure from bottom edge (with or without slight branching near edge)



Case B. Failure from top edge (with or without slight branching near edge)



Case C. Initiation on surface of glass

Case D. Failure at surface on epoxy region (Orientation D)

Figure 3 Surface crack initiation.

All failure loads and failure initiation sites will be entered in the following table below.

Orientation	a	b	c	d	(Circle one)
W [mm] =					Long [mm] =
Lshort [mm] =					t [mm] =
Unit #					Failure Initiation Site Case (A, B, C, D, E, or O)
1					
2					
3					
4					
5					
6					
7					
8					



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N

. | Size: **A** | **METRIC** | Scale: **NONE** |

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## 8. COSMETIC REQUIREMENTS

Cosmetic Specification for Notebook Display, 062-7003E.

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N

□. | Size: A | METRIC | Scale: NONE |

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## 9. REGULATORY

### 9.1. Product Safety (Environmental, Ergonomics, Safety and Health)

Materials: specific chemical composition information or certifications necessary for the product to enter countries, markets, and/or for component(s) material identification, or for to respond to customer requests for information. The information may be in the form of, but is not limited to, Material Safety Data Sheets, material specification sheets, health hazard information, certifications, or other forms of documentation.

### 9.2. RoHS Compliance and other Substance Regulations

This product's components, parts, and packaging shall be manufactured or assembled based upon the following requirements.

10.2.1 The display module must comply with the European RoHS directive, As evidence of such compliance, the supplier must provide a declaration of conformity in accordance with RoHS Declaration of Conformity Procedure, 080-2153.

10.2.2 In addition to RoHS compliance, the display module and its manufacturing process shall comply with Regulated Substances Specification, 069-0135.

10.2.3 The vendor shall provide a written statement declaring the average and maximum amount of mercury in the display module.

### 10.3 Halogen Free

Flat panel display must be must be halogen-free in accordance with the Halogen-Free Specification, 069-1857

### 9.3. Environmental Markings and Recycling

10.3.1 Flat panel display must be modular in design so that parts can be easily separated, without any special tools, for ease of proper recycling/disposal at the product's end-of-life.

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N

□. | Size: A | METRIC | Scale: NONE |

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10.3.2 Flat panel display plastic parts >25 grams must be marked according to ISO 11469 (except for the LGP (light guide panel) and optical films in the backlight).

## 9.4. Product Safety

Flat panel display assembly shall comply with Specification, 069-0279, Product Safety Requirements for Component Flat Panel Display Assemblies.

## 9.5. Ergonomics

The flat panel display must comply with the ergonomic requirements of ISO 13406 parts 1 and 2. The vendor shall provide a written statement that the flat panel display, is certified to comply with ISO 13406, parts 1 and 2.

## 9.6. Electromagnetic Compatibility (EMC)

### 10.6 Emissions

The final product must meet Class B Emission Standards for home electronic device when configured within a system Spec. #062-0718. The display supplier must provide all necessary support as required to meet this requirement. EMI measurements are taken at the worst-case contrast setting.

#### 10.6.1 Susceptibility

Performance degradation due to external noise or RF will be considered as specified in #062-0718 for Class B products.

#### 10.6.2 Spectrum Spreading Compatibility (SSC)

##### 10.6.2.1 Emissions

The final product must be compatible with spectrum spreading conditions specified in 1.2.2 of this document. No failure or degradation in electronic

functionality and optical performance is allowed with the spreading turned ON compared to that when it is turned OFF.

#### 10.6.2.2 Conditions for Spectrum Spreading

Spreading %: 0% (min.), 0.75% (typical), and 1.5% (max.)

Spreading type: center or down

Modulation Rate: 40 to 80 kHz.

## **11 FACTORY/SERVICE REQUIREMENTS**

### **11.1 SQBR**

Factory requirements are outlined in Supplier Quality and Business Requirements, specification 070-1191.

### **11.6 SERVICE REQUIREMENTS**

Service Requirements are outlined in specification 070-0385.

## 12 REFERENCE DOCUMENTS

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□. | Size: A | METRIC | Scale: NONE |

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